IDS

MEG-02-015

June 23, 2005

To: Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject: Serial No. 10/685,872 10/15/03

M.S. Lin

POST PASSIVATION INTERCONNECTION SCHEMES ON TOP OF THE IC CHIPS

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on June 28, 2005.

Stephen B. Ackerman, Reg.# 37761

Signature/Date 6/28/05

The Commissioner is hereby authorized to charge the IDS Processing Fee of $180, under 37 CFR 1.17(p), to Deposit Account No. 19-0033. A duplicate copy of this sheet is enclosed.

U.S. Patent US 2002/0158334 A1 to Vu et al., "Microelectronic Device Having Signal Distribution Functionality of an Interfacial Layer Thereof," discusses a microelectronic device including a microelectronic die having an interfacial metal layer deposited over an active surface thereof to perform a signal distribution function within the device.

U.S. Patent 6,187,680 to Costrini et al., "Method/ Structure for Creating Alumium Wirebound Pad on Copper BEOL," discloses a method for fabricating an integrated circuit (IC) structure having an Al contact in electrical communication with Cu wiring embedded in the initial semiconductor wafer.

U.S. Patent 6,232,147 to Matsuki et al., "Method for Manufacturing Semiconductor Device with Pad Structure," discloses a semiconductor device equipped with secondary pads having adequate arrangement for an arbitrary packaging process.

U.S. Patent 6,229,221 to Kloen et al., "Integrated Circuit Deivce," discloses an integrated circuit device which comprises an active circuit provided in an active circuit area at a surface of a semiconductor body, a plurality of bond pads disposed substantially over th eactive circuit area and electrical connections between the bond pads and the active circuit.

U.S. Patent 6,472,745 to Iizuka, "Semiconductor Device," discloses a semiconductor device in which a plurality of semiconductor chips are consolidated into one and which is provided with at least a set of rerouting wiring lines formed so as to interconnect electrodes of the respective semiconductor chips.

U.S. Patent 6,200,888 to Ito et al., "Method of Producing Semiconductor Device Comprising Insulation Layer Having Improved Resistance and Semiconductor Device Produced Thereby," discloses a semiconductor device comprising an insulation film covering a semiconductor chip so as to expose electrodes or pads fabricated in the chip and wiring lines located on the insulation film and connected to the respective electrodes of pads.

Sincerely,

Stephen B. Ackerman,
Reg. No. 37761

Form PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
MEG-02-015	10/685,872
Applicant: M.S. Lin	
Filing Date: 10/15/03	Group Art Unit:

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	6187680	2/13/01	Costrini et al.	438	688	10/7/98
	6232147	5/15/01	Matsuki et al.	438	108	8/2/99
	6229221	5/8/01	Kloen et al.	257	784	12/6/99
	6472745	10/29/02	Iizuka	257	723	1/14/00
	6200888	3/13/01	Ito et al.	438	597	5/4/00

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

-	U.S. Patent App. Pub. U.S. 2002/0158334 A1 to Vu et al., Pub. Date 10/31/02, Filed 4/30/01, U.S. Cl. 257/723.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.